operating characteristics of the resultant semiconductor device are adversely affected. Specifically, a reduction in the contact area between the contact plug 16 and the conductive line 18 increases the contact resistance, thereby reducing the operating speed of the semiconductor device.

Please rewrite the paragraph on page 6, lines 1-9, to read as follows:

Next, referring to FIGS. 4A and 4B, a second interlayer dielectric layer 36 is formed on the entire surface of the semiconductor substrate 30 on which the conductive line 34 has been formed. The second interlayer dielectric layer 36 may be a silicon oxide layer, a silicon nitride layer, a silicon oxynitride layer, a USG layer, a BSG layer, a BPSG layer, a PE-TEOS layer, a TEOS layer or an O_3-TEOS layer. If the upper surface of the second interlayer dielectric layer 36 is not flat, the entire surface thereof can be planarized by a method appropriate to the material thereof, e.g., a chemical mechanical polishing (CMP) method, an etch back method, or a thermal reflow method.

Please rewrite the paragraph on page 7, lines 10-17, to read as follows:

The etching of the second interlayer dielectric layer 36 preferably stops at the upper surface of the conductive line 34. In this case, the portions 40 of the second interlayer dielectric layer on the left and right sides of the conductive line 34 are exposed, as shown in FIG. 5A, because the first width W_1 is larger than the critical dimension D of the conductive line 34. For reasons that will be described in more detail

later on, in the first embodiment of the present invention, the finally formed self-aligned contact is to have a width no smaller than the critical dimension D of the conductive line 34.

Please rewrite the paragraph on page 10, lines 3-22, to read as follows:

Referring to FIGS. 9A and 9B, a conductive material is deposited in the contact hole 42 and on the second interlayer dielectric layer 36 to form a conductive layer. Here, the inclined sidewalls of the second interlayer dielectric layer 36 provide an improved step coverage of the conductive layer and prevent defects, such as voids, from occurring. Subsequently, the upper surface of the semiconductor substrate on which the conductive layer has been formed is planarized by CMP or an etch back method. The conductive layer can be an aluminum layer, a copper layer, a gold layer, a silver layer, an impurity-doped polysilicon layer, a tungsten layer, a platinum layer, a tungsten silicide layer, a titanium silicide layer or a combination of the above-mentioned layers. Preferably, the planarization stops when the upper surface of the conductive line 34 is reached. The contact plug 44 connecting the conductive line 34 to the conductive region 31 is formed once the upper surface of the conductive line 34 is exposed by the planarization process. The contact plug 44 is thus a self-aligned contact formed between the conductive line 34 and the conductive region 31. Note, before the conductive layer is formed, a barrier metal layer (not shown) may be formed to improve the adhesiveness between the contact plug 44 and the first interlayer dielectric layer 32